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IN THE SPECIFICATION

Please replace the paragraph beginning on page 5, line 9 with the following paragraph:

The functional block diagram of Figure 1 illustrates a cell stream replicating device 10 according to the preferred embodiment which is connected between an ATM traffic generator 12 and a multiple input port ATM data communication device 14, such as an ATM cell switching device. The ATM traffic generator 12 produces an ATM cell stream, such as shown at ref. no. 54 in Figure 2, on physical interface/line 16 (Figure 1). The cell stream 54 carries a traffic pattern used for testing purposes such as performance testing. As noted from Figure 2, the ATM cell stream 54 is "continuous" in the sense that even if there is no user information or data payload being carried by the cell stream at any given point in time (i.e. other than the ATM control information encapsulated in the cell header which is required for the functioning of the cell stream itself), the ATM traffic generator 12 generates idle or unassigned ATM cells 53 as known in the art, such that there are no gaps or discontinuities in the cell stream. Test generator 12 is commercially available from a variety of sources, including the Interwatch 95000 (trademark) model by GN Nettest and the AX4000 (trademark) model Adtech.

Please replace the paragraph beginning on page 7, line 9 with the following paragraph:

Figure 3A is a system block diagram illustrating a first system for carrying out the preferred embodiment in practice. In this system, the cell stream replicating device 10 comprises a microprocessor 30 and an associated memory 32 which may be internal to (e.g., a high speed cache memory) or external of the microprocessor 30. The input port 18 is a serial port which converts a bit stream into corresponding word data readable by the microprocessor 30. The input port 18 is connected to the microprocessor 30 via an interrupt signal 34. The microprocessor is

also connected to output ports 28 through various means well known in the art. In this case, the output ports 28 are serial ports which convert word data provided by the microprocessor 30 into a serial bit stream.

Please replace the paragraph beginning on page 7, line 19 with the following paragraph:

In the illustrated embodiment, memory 32 is organized into N physical FIFO buffers 27 such that each logical buffer 26 corresponds to one of the physical buffers 27. The microprocessor 30 implements the broadcast means 20, a portion of the delay means 24, and the scheduling means 25 by executing a program which, upon receipt of a new cell from the input port 18, copies the new cell to each physical buffer 27. The program also determines when any of the physical buffers 27 are full, and, for those buffers which are full, forwards the lead cells stored therein to the corresponding output ports 28. A housekeeping function of the program maintains each physical buffer by discarding cells which have been transmitted. For example, the physical buffers 27 may be constructed as linked lists, the lead elements of which are discarded when the data is forwarded to the output ports 28.

Please replace the paragraph beginning on page 9, line 23 with the following paragraph:

In order to accommodate this function, the scheduling means 25 according to this alternative embodiment forwards the data payload of the ATM cells stored in the logical buffers 26 to the SAR interface devices which function as output ports 28 (as opposed to forwarding the entire ATM cell, inclusive of header, to the serial ports of the preferred embodiment). In addition, the modified scheduling means 25 sends the channel and other control information